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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Gabriele Manganaro

Application No.: 10/672,061

Group Art Unit: 2816

Filed: September 26, 2003

Examiner:

Confirmation No.: 4728

Title: METHOD AND APPARATUS FOR ROBUST BIASING OF BIPOLAR  
AND BiCMOS DIFFERENTIAL ARCHITECTURES

CERTIFICATE OF MAILING OR TRANSMISSION	
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Date	Signature
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Typed or printed name of person signing certificate	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This Information Disclosure Statement is submitted:

☐ under 37 CFR 1.129(a), or  
(First/Second submission after Final Rejection)

☒ under 37 CFR 1.97(b), or  
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits in a non-provisional application, including a CPA, or a Request for Continued Examination).

☐ under 37 CFR 1.97(c) together with either:  
☐ a Statement under 37 CFR 1.97(e), as checked below, or  
☐ a \$180.00 fee under 37 CFR 1.17(p), or  
(After the 37 CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:  
☐ a Statement under 37 CFR 1.97(e), as checked below, and  
☐ a \$180.00 fee under 37 CFR 1.17(p), or  
(Filed after final action or notice of allowance, whichever occurs first, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):  
Applicant requests that the IDS and cited reference(s) be placed in the application filewrapper.  
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

- ☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or
- ☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)

Applies to original applications (other than design) filed on or after May 29, 2000

- ☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.
- ☒ Enclosed herewith is form PTO-1449:
  - ☒ Copies of the cited references are enclosed.
    - ☐ Since this application was filed after June 30, 2003, copies of issued U.S. patents and published U.S. applications are not required and are not being provided.
  - ☐ Copies of the cited references are enclosed except those entered in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed. [The earlier application contains copies of the cited references.]
  - ☐ The listed references were cited in the enclosed International Search Report in a counterpart foreign application.
  - ☐ The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:
    - ☐ the explanation provided on the attached sheet.
    - ☐ the explanation provided in the Specification.
    - ☐ submission of the enclosed International Search Report.
    - ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
    - ☐ the enclosed English language abstract.

☐ Applicant requests that the following non-published pending applications be considered:

Examiner's  
Initials

\_\_\_\_ U.S. Patent Application No. [     ], by [inventor(s)], filed [     ], Docket No.: [     ]  
\_\_\_\_ U.S. Patent Application No. [     ], by [inventor(s)], filed [     ], Docket No.: [     ]  
\_\_\_\_ U.S. Patent Application No. [     ], by [inventor(s)], filed [     ], Docket No.: [     ]

\_\_\_\_\_  
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Date

- ☐ A copy of each above-cited application, including the current claims, is enclosed.
- ☐ A copy of each above-cited application, including the current claims, is enclosed, except those entered in prior application, U.S. Application No. [     ], to which priority under 35 U.S.C. 120 is claimed.

The Examiner is requested to return a copy of the above list of pending applications indicating which references were considered with the next office communication.

It is requested that the information disclosed herein be made of record in this application.

Method of payment:

- ☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply. A copy of this Statement is enclosed.
- ☐ Please charge Deposit Account 08-0380 in the amount of \$[     ]. A copy of this Statement is enclosed.
- ☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By Carol M. Fleming  
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Concord, MA 01742-9133

Dated: 5/20/04

PTO-1449 REPRODUCED

**INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION**

May 20, 2004

(Use several sheets if necessary)

 ATTORNEY DOCKET NO.  
3226.1016-001

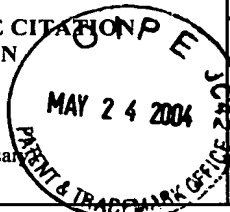
 APPLICATION NO.  
10/672,061

 FIRST NAMED INVENTOR  
Gabriele Manganaro

 FILING DATE  
September 26, 2003

EXAMINER

 CONFIRMATION NO.  
4728

 GROUP  
2816

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

AR	Gray, P. R. and Meyer, R. G., "Analysis and Design of Analog Integrated Circuits, 3rd Ed.," pp. 236-241, John Wiley & Sons, Inc., New York, 1977.
AS	Mizuno, M., et al., "A 3-mW 1.0-GHz Silicon-ECL Dual-Modulus Prescaler IC," <i>IEEE Journal of Solid-State Circuits</i> , 27(12): 1794-1798, (1992).
AT	A. M. Niknejad, J. L. Tham, and R. G. Meyer, "Fully-Integrated Low Phase Noise Bipolar Differential VCOs at 2.9 and 4.4 GHz," Proceedings of the 25th European Solid-State Circuits Conference, 1999. pp.198-201. <a href="http://rfic.eecs.berkeley.edu/~niknejad/publications.html">http://rfic.eecs.berkeley.edu/~niknejad/publications.html</a>
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